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Term (Index)	Definition
overlay	superposition of the pattern on the mask to the patter previously created on the surface of the wafer.
alignment	positioning of the mask (or reticle) in lithographic processes relative to a wafer prior to exposure of the resist.

 Back

The Fundamentals of Overlay Metrology

Neal T. Sullivan, Technology Development Group, Schlumberger ATE/VS, Concord, Mass. -- *Semiconductor International*, 9/1/2001

At a Glance

An overview of the basics of overlay metrology, including process and measurement error sources.

Overlay metrology equipment historically has had little difficulty meeting state-of-the-art process error budgets through the 0.25 µm technology node. In fact, typical overlay measurement equipment performance has been better than metrology error budget allocations by 20-30%.[1] This can be ascribed to several factors. First is the lavish error budget, compared with critical dimension (CD) metrology (3% of minimum design rule vs. <1% for CD metrology). The second is the relative stability of the overlay measurement target design, which typically doesn't scale (in the wafer plane) with each process generation, thereby presenting similar measurement issues for each successive process generation.

Finally, this historic ease of meeting process error tolerance can also be attributed to the lack of a clear connection to device yield. For CD measurements, clear relations to circuit performance and cost are used to derive specific process control limits.[2] In the case of overlay metrology, the correlation to final device yield is a much more complex combination of factors and, as such, is much more difficult to determine.

Semiconductor pattern overlay is the measure of vector displacement from one process level (substrate) to another level (resist), usually separated by an intermediate (thin-film) layer. The overlay requirements for a particular device design are typically determined through a combination of CD and overlay excursions.

This is shown schematically in Figure 1, where

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- Web Connection

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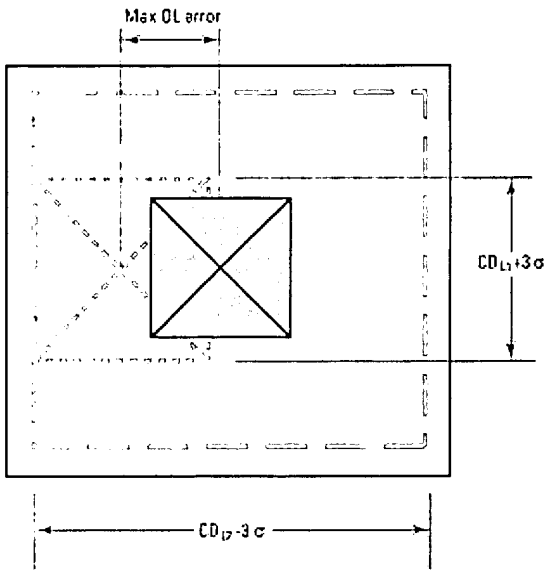
DESIGN RULE GENERATION SCHEMATIC



1. The maximum allowable overlay shift shown as the center-to-center distance.

the shaded square represents one level and the open square represents the second level.[3] In this example, the level-one critical dimension (CD_{L1}) is increased by the maximum tolerance (3 σ), and the level-two critical dimension (CD_{L2}) is reduced by the maximum tolerance (3 σ). The maximum allowable overlay shift, while maintaining level one (dark box) completely within level two (light box) — the design rule for this example — is shown as the center-to-center distance.

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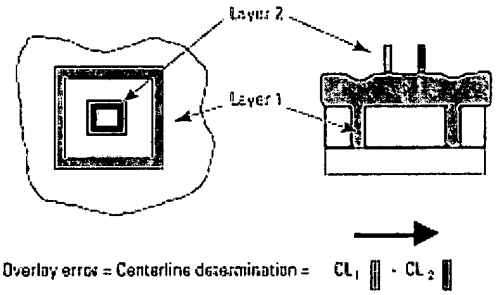
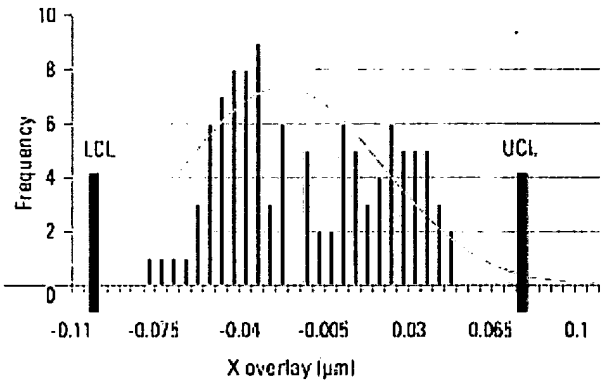
OVERLAY MEASUREMENT TEST STRUCTURE



2. A box-in-box test structure is commonly used to measure overlay error.

in-box test structure (Fig. 2) and is defined as the planar distance from the center of the substrate target (outer green box) to the center of the resist defined target (inner blue box). Overlay measurement involves the determination of the centerline of each structure along both the X and Y axes. Centerline determination utilizes the symmetry around the structure's center such that the error associated with edge determination will tend to cancel from each side of the structure. Conversely, in a linewidth determination, the error associated with each edge combines in an additive fashion.

PLATYKURTIC OVERLAY DISTRIBUTION



3. A typical example of the non-normal nature of the raw overlay measurement results.

Overlay measurement uncertainty is a complex function of tool, target and process interactions, and is difficult to quantify. The device overlay tolerance specification is derived from the technology design rules. The circuit performance requirements are compared with established manufacturing tolerances. All error sources — from the mask to the measurement uncertainty — are combined either linearly (most conservative) or are added in quadrature (for Gaussian error distributions) to calculate the overlay tolerance. Successful process control of 0.35 µm process technology was possible through initial stepper/scanner matching and subsequent control of layer-to-layer overlay through the use of X and Y offsets. Process tolerances for the 0.35 µm generation, typically 100 nm on critical levels, were generous enough that the non-normal (multi-modal) behavior and dependence on location within a field did not affect the ability to meet target performance specifications. A typical example of the non-normal nature of the raw overlay measurement results is shown in Figure 3. It is readily apparent from the figure that the actual data distribution is multi-modal and platykurtic.[4] This form of the data distribution is due to systematic lithography errors.

Product misregistration overlay budgets for current 0.18 µm production process technologies, however, are <70 nm. To consistently achieve these levels of performance, every aspect of overlay error must be identified and corrected. To that end, modeling is employed to correct the systematic

sources of overlay error. Process control is more difficult unless these systematic errors can be accounted for, because their presence distorts the observed nature of the variation.

Process error sources

The sources of overlay error attributable to the wafer stepper/scanner generally arise from the lens (intrafield) and the stage (grid). Intrafield errors can be further broken out into errors that either are intrinsic to the optics of the stepper/scanner (distortions) or are derived from interactions of the reticle with the stepper/scanner's optical subsystem.

The former set of errors are characteristic of a given lens and are typically addressed during lens manufacture (direct control over a wafer stepper/scanner to control intrinsic lens distortions is not available). The residual lens distortions are accommodated for, at the price of individual stepper/scanner overlay performance, in the process of stepper/scanner matching. Therefore, it is essential that each new lens be thoroughly characterized with respect to distortion because these errors are an integral part of the performance of the stepper/scanner in manufacturing.

Equation 1 is a mathematical model for all X direction intrafield error terms associated with stepper (a similar equation applies for the Y direction).[5]

$$\delta x = \alpha + (\delta M/M)x_0 - \theta y_0 - t_1 x_0^{\,2} - t_2 x_0 y_0 - \quad (1)$$

$$Ex_0(x_0^{\,2}+y_0^{\,2}) + Fx_0(x_0^{\,2}+y_0^{\,2})^2 + \text{Residuals}$$

From Equation 1, the terms up to first order in x — offset (α), magnification (δM/M) and rotation (θ) — can typically be controlled from the stepper/scanner. The higher-order terms, trapezoid (t_1 and t_2), third (E) and fifth (F) order distortions are not easily controlled (trapezoid) or are intrinsic to the stepper lens (third and fifth order).

Stage-derived errors may also be divided into those over which the process engineer has control and those that are intrinsic to the mechanical subsystem. As shown in Equation 2, the systematic grid errors are very similar in mathematical form to the intrafield or lens errors shown in Equation 1.[6] But, unlike the intrafield case, the terms apply across the entire wafer.

$$\delta x = \alpha + (\delta M_g/M_g)x_0 - \theta_g y_0 + y_0^{\,2} Dx +$$

Residuals (2)

$\delta M_g/M_g$ is the wafer scaling coefficient, U_g is the wafer rotation coefficient and D is the stage bow coefficient.

Typically, the stepper will allow direct control over only the scale and rotation terms. Accurate separation of the various error components shown in Equations 1 and 2 is heavily dependent upon both sample plan and model statistics. When establishing the metrology sample plan, it is important to maximize symmetry and spatial coverage. These concepts derive from an understanding of the systematic error components due to the lithography tool. To achieve symmetry, die and intrafield site positions should be chosen so that they are balanced by an opposite die or site (not necessarily within the same field location). For good spatial coverage, measurement locations must be positioned such that they adequately cover the area of interest (wafer or die) in both the X and Y directions. Poor symmetry can lead to incorrect systematic error assessment.

In the extreme intrafield case — one site per field — magnification error will appear as a translation error. Correction of this through an offset term will result in a 2× error at opposing die locations. Poor spatial coverage will also lead to incorrect systematic error assessment. For example, sampling the field in the four corners only will result in exaggerated field magnification terms. This is due to the

inclusion of (non-correctable) higher-order (third and fifth) distortion terms. In this instance, adding one or two sites along the die edge (at X=max, Y=0 or X=0, Y=max) will allow for differentiation of the higher-order systematic errors from magnification terms.

Error sources

Overlay measurement must be sensitive enough to discriminate error components derived from all sources. So it is critical that the contribution of the measurement tool to the total error be minimized and well controlled for all process levels.

Overlay measurement difficulties arise in manufacturing from an interaction of the measurement equipment with the instance of the measurement feature (process variations and target design), primarily due to low edge contrast. Low-contrast edges often result from advanced planarization techniques such as chemical mechanical polishing (CMP), used to accommodate a decreasing photolithography process window. These problems require that implementation of overlay metrology be performed with a deeper understanding of the physics of the measurement instrument and the interaction of the process module with the overlay measurement target. In effect, the sample must be considered to be an optical element of the measurement system.

The inherent, tool-limited measurement accuracy is commonly referred to as tool-induced shift (TIS).[7] TIS is quantified by measuring the same feature at 0 and 180° (wafer) rotations. TIS is half the sum of the measurements from each orientation. TIS error arises from optical alignment, illumination and aberrations of the system optics. TIS interacts with process conditions, achieving different values for different resist thicknesses, substrate surface roughness, substrate topographies and structure designs.[8]

While it is generally true that minimum TIS results in best overall metrology performance, it is also clear that there is a complex interaction between the various measurement schemes (optics, algorithms, illumination, etc.) and TIS performance on a given substrate. TIS is a very complex function of choice of focus method (e.g. single vs. double grab), optical configuration, and substrate material. It is not possible to accurately predict the TIS response for a given instrument on a new substrate based only on an empirical understanding of the instrument's performance on other materials.

Overlay measurement accuracy errors, if not recognized and accounted for, can produce false systematic stepper/scanner errors. The introduction of systematic measurement errors into a simulated stepper setup data set results in the transposition of those errors to the stepper.[9] TIS shows up in the translation term of the modeled stepper systematic errors, and pixel scale directly modifies the grid and field magnification (scale) coefficients. If these errors are not properly ascribed to the metrology tool, they will end up as a stepper/scanner input correction, which will further degrade product overlay performance. It is important to accurately quantify and assign the contribution of the measurement tool's error component to the measured value, and to minimize its impact via a hardware modification (e.g. optical alignment/columnation) or software calibration.

The final component of the measurement contribution to the overlay error comes from the measurement precision of the tool. This component is easily quantified by performing repeated measurements of a sample in a carefully designed analysis of variance experiment. All of these sources of measurement error combine to constitute the total measurement uncertainty.

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Product Release

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Micro-Metric launches Innova 200

Date announced: 29 Jul 2003

Micro-Metric has a new, exceptionally accurate system for automated semiconductor overlay and linewidth measurement. Based on the company?s extensive background in precision dimensional metrology, the Innova 200 is a cost-effective solution to verify the alignment between layers on shrinking wafer geometries.

Innova 200 is unique in that it measures both linewidth and overlay dimensions, making it particularly effective in determining overlay alignment. The system creates an intensity profile of the overlay pattern in X and Y directions. Any pair of edges in the profile can be measurement targets. The centerline between these two measurement targets is determined for both the inner box and outer box; the difference between the two centerlines (in X and Y directions) constitutes the overlay measurement.

INNOVA 200 offers several important features:

Automatic wafer handler with prealigner, motorized nosepiece, and pattern recognition. Wafers can be loaded from and returned to any slot in either of two cassettes. The prealigner can align to flats of all sizes, or notches. The system automatically deletes alignment marks, and performs measurements without operator assistance

User-definable operating software: application programs included with Innova 200 are written using Micro-Metric?s powerful Measurement Control Language (MCL). Program files are easy to read, and allow users to modify existing programs to control the system.

Statistical data analysis: Innova 200 processes measurement results to determine the average, maximum, minimum, spread, standard deviation, and other statistical results from selected sets of data. Results are displayed on screen, printed as reports, saved to a file, or transferred directly to a statistical database.

Overlay measurement accuracy is 0.005 microns or less. Overlay measurement repeatability is 0.005 microns or less at 3 Sigma. Positioning resolution is 0.01 microns (10 nm). Velocity is 75 mm/sec. (3 in./sec.).

Innova 200 also measures a wide range of critical dimensions on wafers, such as linewidths, contacts, vias, circles, arcs, and other features ranging from 0.5 to 800 microns. The system can also be operated manually.

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